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Introduction

These Guidelines set out best practice to reduce the cost of your boards and to minimize the risk of errors arising during manufacture.

There is no general consensus throughout the global PCB industry on terminology, so if we feel any term we use may be unclear we have tried to explain it when it first appears.

Input data formats

Accepted data formats for PCB layout data are:

Preferred

Artwork:

- Gerber RS-274X (Extended Gerber with embedded apertures - developed by Gerber Systems)

Artwork means all copper layers, soldermask and legend layers, board outline or mechanical layer, SMD pasta layers, etc.

Drilling:

- Excellon (1 or 2) + appropriate tool list (ideally embedded)
- Sieb&Meyer + appropriate tool list (ideally embedded)
- Gerber format RS-274X or RS-274D (only true drill data, no drillmap)

IMPORTANT:

Please supply **ONLY ASCII**-encoded files. These files are man-readable so that our engineers can check them visually if needed during data preparation. So we don't accept formats such as EIA or EBCDIC.

Accepted

Eagle .BRD files are accepted BUT we still recommend to generate the gerber and excellon files at the CAD system of the customer. Generating the gerber data and excellon data by the customer minimizes the risk of conversion errors that could arise if different versions of eagle are used to design and generate the gerber and excellon dataset. Check "Generating Gerber & Excellon data files in Eagle" at page 16.

NOT ALL CAD PCB design data is ACCEPTED!

We **do not accept any CAD PCB design data besides the Eagle .BRD file.**

1. Converting CAD data into production data may lead to errors which we cannot cross-check
2. It is impossible to have legal copies of every CAD PCB design package in the market and to have the necessary knowledge to use them all correctly. As designers do not all use the same software version, we would need to have a whole range of update patches as well.

Gerber is clear and unambiguous. It has been the industry-standard format for PCB manufacture for many years. Every PCB design package can output Gerber data and the process will be fully described in your CAD PCB design package handbook or help-files.

You can check the accuracy of the Gerber output data by downloading one of the many free Gerber viewers available on the internet. We recommend GC-Prevue available as freeware from www.graphicode.com.

Input data requirements

1. **Preferred** data formats are:
 - For Artwork -- Extended Gerbers (RS-274X)
 - For Drilling -- Excellon1 + appropriate tool list (ideally embedded)
2. **Provide us ONLY** with the data files needed for production. These are:
 - Gerber files for the copper layers, soldermask and legend layers, mechanical layer and SMD paste layers.
 - Excellon drill file(s) for drilling.

Please DO NOT provide any additional files such as original CAD data, Graphiccode GWK files, PDF files, Word files (doc), Excel files (xls), part lists, placement and assembly information, etc.

Where possible check your generated output data (Gerbers & Excellon) with a Gerber viewer before you send it on to production. Make sure that all instructions or other necessary input needed for making the boards are included in the Gerber and Excellon files.

3. Use clear and easy to understand file naming and try to avoid long filenames. Make sure that we can easily determine the layer function from the filename.

Good file naming:

Name	Name	Size	Type
SMALLTCSV2BALE.BOT	141101-A_SOLDERMASK BOTTOM.GBR	3 KB	GBR File
SMALLTCSV2BALE.SMB	141101-A_SILKSCREEN TOP.GBR	10 KB	GBR File
SMALLTCSV2BALE.SMT	141101-A_SILKSCREEN BOTTOM.GBR	2 KB	GBR File
SMALLTCSV2BALE.TOP	141101-A_SIGNAL TOP.GBR	3 KB	GBR File
SMALLTCSV2BALE.DRD	141101-A_SIGNAL BOTTOM.GBR	10 KB	GBR File
SMALLTCSV2BALE.SST	141101-A_DRILL PROGRAM.GBR	3 KB	GBR File
SMALLTCSV2BALE.DTS	141101-A_SOLDERMASK TOP.GBR	3 KB	GBR File

File naming is too long, not advisable:

Name	Name	Size	Type
cam_unit_lamp_led_guide-Master Design(Stencil top).gbr		1 KB	GBR File
cam_unit_lamp_led_guide-Master Design(solder mask top).gbr		2 KB	GBR File
cam_unit_lamp_led_guide-Master Design(solder mask bottom).gbr		6 KB	GBR File
cam_unit_lamp_led_guide-Master Design(Silkscreen Top).gbr		210 KB	GBR File
cam_unit_lamp_led_guide-Master Design(silkscreen bottom).gbr		14 KB	GBR File
cam_unit_lamp_led_guide-Master Design(drills plated).drl		1 KB	DRL File
cam_unit_lamp_led_guide-Master Design(drill unplated).drl		3 KB	DRL File
cam_unit_lamp_led_guide-Master Design(Bottom).gbr		10 KB	GBR File
cam_unit_lamp_led_guide(CAMPlot).txt		9 KB	Text Document
cam_unit_lamp_led_guide-Master Design(Top).gbr		5 KB	GBR File

Bad file naming: no info on layer function in the file names:

Name	Name	Size	Type
	filter_v1_0.inf	4 KB	Setup Information
Layer_1.gbr	filter_v1_0.gb4	3 KB	GB4 File
Layer_3.gbr	filter_v1_0.gb3	2 KB	GB3 File
Layer_4.gbr	filter_v1_0.gb2	10 KB	GB2 File
Layer_5.gbr	filter_v1_0.gb1	5 KB	GB1 File
Layer_6.gbr	filter_v1_0.gb0	1 KB	GB0 File
Layer_7.gbr	filter_v1_0.drl	2 KB	DRL File

4. **DO NOT scale** your data. All data provided must be scale 1/1 (100%).
5. Make sure that your Gerber files DO NOT contain apertures with a zero-size (size = 0.00mm) and that your Excellon data DOES NOT have zero-sized tools (size=0.00mm).

- Use the same offset for all your Gerber layers and the Excellon drill data. Preferably use no offset at all.



- Use the same units (mm or inch) in your Gerber & Excellon output files as in your CAD PCB design software. This will eliminate conversion or rounding errors.
- Use the same resolution (grid) for your Gerber & Excellon data to allow a perfect match.

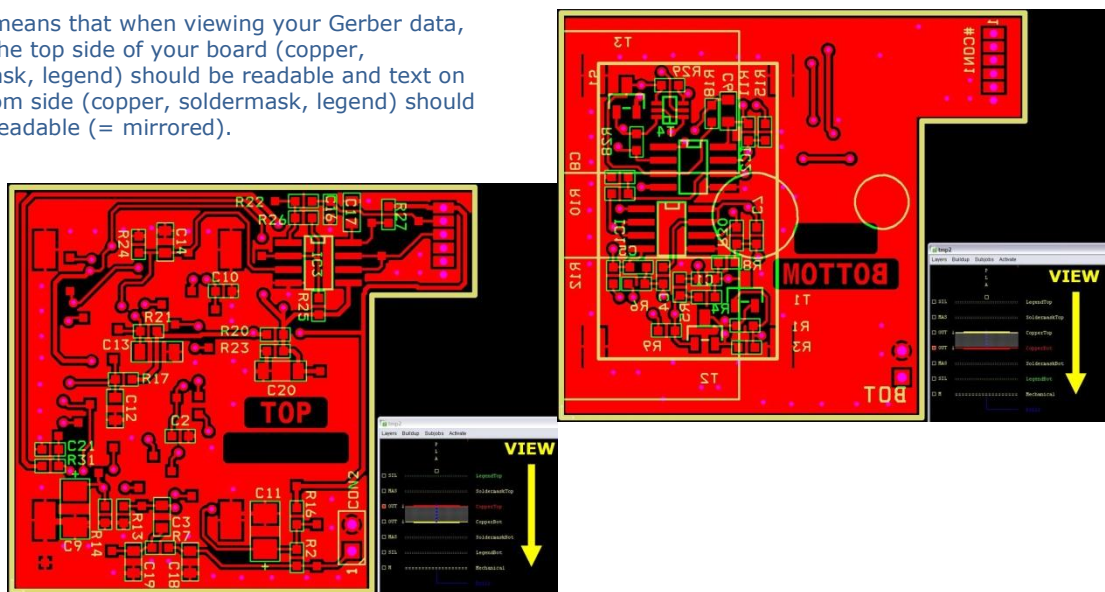
Also make sure that the resolution (grid) used for your output (Gerber & Excellon) is at least a factor 10 better than the resolution (grid) used in your CAD PCB design software.

Example: If you use a 10 mill resolution to draw your board in your CAD PCB design software, then use a 1mil output resolution for your Gerber & Excellon output.

- Make sure that your data is supplied as **seen from top to bottom through the PCB**. **DO NOT mirror** (or reflect) any data layer – image or drill.

Viewing a PCB from top to bottom through the board is the universal practice in the PCB industry. We view and handle your data in that way, as does your CAD PCB design software.

-> This means that when viewing your Gerber data, text on the top side of your board (copper, soldermask, legend) should be readable and text on the bottom side (copper, soldermask, legend) should be non-readable (= mirrored).



10. Put some small text (board identification, company name, etc...) in the copper layers. Make sure the text complies with the readability rules. This will help us to avoid mirroring errors.
11. RECOMMENDATION. In your Gerber files use flashed pads as often as possible.
12. RECOMMENDATION. In your CAD PCB design software try to create an aperture list for Gerber output which only shows the apertures used in the design.
13. Make sure that you include the board outline on all layers. This will enable us to properly align all layers in case of an offset problem. Also include the board outline in a separate Gerber mechanical plan.

Classification

Introduction.

We use "pattern classes" and "drill classes" as a convenient shorthand to measure the manufacturability of the PCB. This controls whether the board can be made in our Elektor PCB Service.

The pattern class covers

- the minimum sizes for copper track (conductor) and gap (isolation) (TT = Track to Track , TP = Track to Pad, PP = Pad to Pad and TW = Track Width)
- the minimum copper rings on outer and inner layers (OAR = Outer Annular Ring, IAR = Inner Annular Ring)
- the minimum IPI (Inner-Layer Pad Isolation) is the clearance between any copper part on an inner layer and the copper edge of a Plated Through Hole.

The smallest of these values determines the pattern class.

The drill class is based on the smallest Tool size on the board.

For more information [see the current Classification table](#).

IMPORTANT: Annular Ring calculations are done from the production TOOLSIZE for the holes, not from the finished hole ENDSIZE. --> For the conversion rules for ENDSIZE to TOOLSIZE see Holes section 6.

1. The Classification table shows the lower limit values of any given class.
2. The Annular Ring values OAR and IAR in the classification table are for plated holes (PTH). For connected non-plated (NPTH) holes we recommend a minimum annular ring of 0.30 mm. As NPTH holes have no plated barrel, a smaller annular ring may lift during soldering or break away even during normal operating conditions.
3. RECOMMENDATION. Do not design up to the limits of any given classification. Always keep a small margin above the classification limits. This may be needed where the CAD output does not exactly match the design data due to rounding or matching errors caused by different units or grids (see section Input data requirements points 7 & 8)

Holes

1. Tool lists for drill files are **ALWAYS** read by our CAM systems as finished hole sizes (ENDSIZE).
2. All PCB drills are manufactured in increments of 0.05 mm. So we convert the drill sizes given in the drill files or tool lists into millimeters and round up to the nearest 0.05mm.

For example:

- Drill size of 31mil is converted to 0.7874mm and then rounded to 0.80mm.
- Drill size of 32mil is converted to 0.8128mm and then rounded to 0.80mm.
- Drill size of 33mil is converted to 0.8382mm and then rounded to 0.85mm.

3. If possible, provide separate drill files for plated (PTH) and non-plated (NPTH) holes. If this is not possible, always specify different tools for PTH and NPTH holes and mark clearly which tools are PTH and which tools are NPTH.

4. When no PTH/NPTH info is given we use the following rules to determine PTH/NPTH:

For 2-layer and multilayer boards: → ALL holes are considered PTH except the following cases which are considered NPTH:

- Non-connected holes without copper pads.
- Non-connected holes where the copper pad size is equal to or smaller than the drill TOOLSIZE (the copper pad will be removed in single image preparation)
- Connected holes with a copper pad on 1 side (outer), no connection on any other layer (outer or inner) and no copper pad on the other side (outer).

5. Finished hole sizes (ENDSIZE) smaller than or equal to 0.45mm are by default considered as VIA holes.

IMPORTANT:

This default via-rule affects:

- Finished hole size to production drill size (ENDSIZE to TOOLSIZE) conversion
- The standard tolerance on via hole ENDSIZE diameter.

6. To allow for the plating in the hole we drill holes prior to plating at a larger size (drill over-sizing) The conversion rules from finished hole ENDSIZE to production TOOLSIZE are:

TOOLSIZE = ENDSIZE + 0.10mm for vias (= ENDSIZE ≤ 0.45mm)
 + 0.15mm for Plated Through Holes (PTH) (= ENDSIZE ≥ 0.50mm)
 + 0.05mm for Non Plated Through Holes (NPTH)

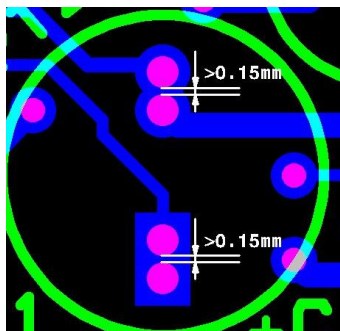
7. Standard tolerances on drill ENDSIZE diameter.

NPTH holes	+/- 0.05mm
PTH holes	
ENDSIZE ≥ 0.50mm	+/- 0.10mm
ENDSIZE ≤ 0.45mm	+0.10/-0.30mm

8. Drilled holes must not overlap the board contour, except for
- NPTH holes without copper pads: these NPTH holes will be treated as part of the board outline.
9. Overlapping drill holes.

Do not overlap drill holes. These cause broken drill bits and small remaining material parts may cause plating voids in production.

The minimum drill hole to drill hole distance is 0.15mm (=measured edge to edge of drill TOOLSIZE).



10. Annular Rings on oblong pads.

The rules for annular rings on oblong pads are **NOT** different from round pads, but we allow some exceptions to the rules.

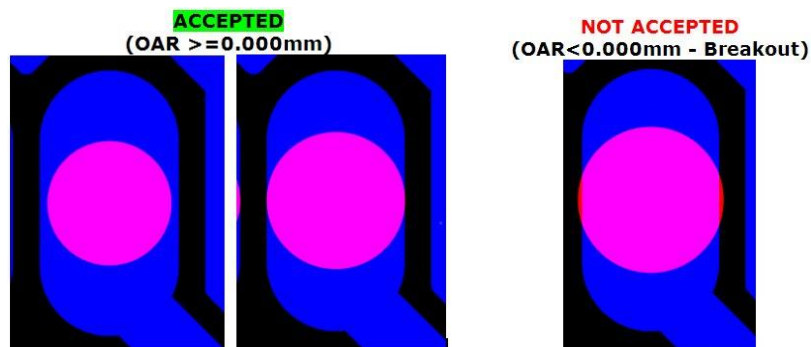
Oblong pads with NPTH drills:

- MUST ALWAYS FULLY COMPLY with the standard Annular Ring rules for any given pattern class.
- The recommended Annular Ring for any NPTH hole is 0.30mm (see section Classification – point 2)

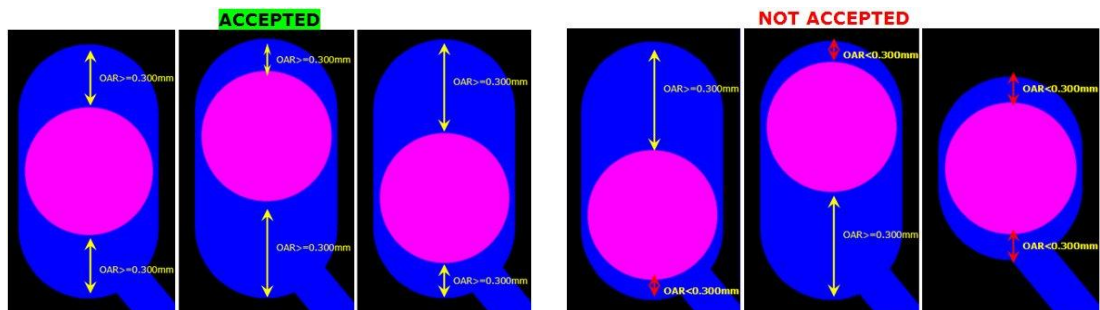
Oblong pads with PTH drills

The measurements below are taken from the production TOOLSIZE.

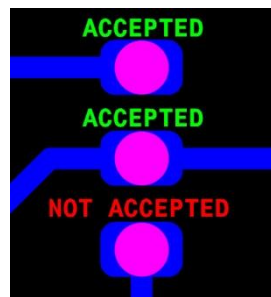
- On the **smallest side** of the oblong pad the **OAR must be $\geq 0.000\text{mm}$** (i.e. no breakout is allowed)



- On the **longest side** of the oblong pad **in both directions** the **OAR must be $\geq 0.300\text{mm}$** (but the hole need not be in the centre of the pad)



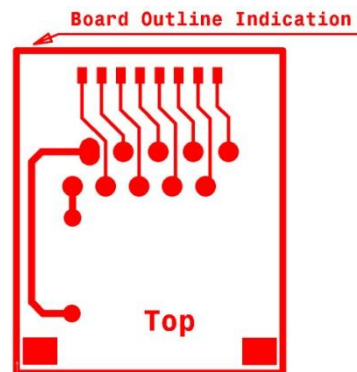
- Any risk that the drilling could disconnect the pad from the track is inadmissible.



Copper layers

1. When generating output, use “flashes” for pads and avoid “painted” pads (i.e. pads filled with small draws)
2. Avoid filling large copper areas or copper planes with small draws (“painting”). Where possible, use contours or polygons to construct areas or planes. Contourized areas or Polygon Area fill are standard features in Extended Gerber output (RS-274X).
3. When generating output include the board outline in your copper layers.

This is best done using a small line (e.g. 0.50mm wide) where the center of the line is the exact board outline. We will remove this line during the making of the production tools.



4. Remove copper pads from NPTH holes if these pads are not used or connected to other copper. If you require copper pads on NPTH holes then it is advisable to use a minimum Outer Annular Ring (OAR) of 0.30mm (see Classification point 2).
5. Check your final design for small areas of unconnected copper or narrow copper webs and slivers which can lead to problems in production.



X: Must meet classification criterion for minimum Track Width (TW).

A: Avoid if possible.

B: Preferred design

6. Minimal clearance between edge of board and pattern.

For routed boards:

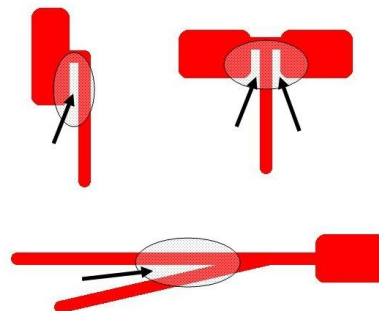
- 0.25mm on outer layers
- 0.40mm on inner layers

Any text placed in a copper layer has to comply with the design rules for the given class (see classification table).

All copper text must be correctly readable. As a **PCB is always viewed from top to bottom through the PCB**, text on the top layer of your board should be readable and text on the bottom layer should be non-readable or mirrored.

7. Avoid “peelables”.

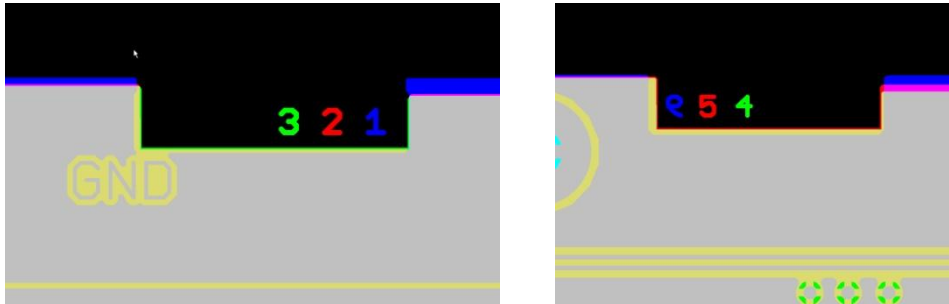
“Peelables” occur during production and are small/narrow pieces of photo resist enclosed by pads, traces and/or planes which may “peel” away during processing and cause short or open circuits. All copper even within the same net must comply with the design rules for the given class (see classification table).



8. ALWAYS provide the proper layer sequence for a multilayer board.

The layer sequence can be given in several ways:

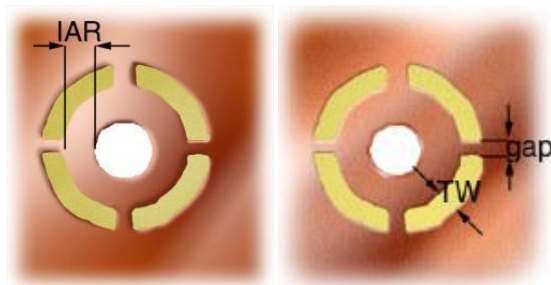
- Indicate the layer numbers in the copper image by placing a logical number in each layer (1 for top layer, 2 for inner1, 3 for inner2, etc...). Make sure the numbers are positioned in such a way that they do not overlap, and can be seen through the complete PCB.



- Name each layer file in a way which indicates clearly the sequence to be used (e.g. T(op), I(nner)1, I(nner)2, B(ottom)).
- Include in your Gerber mechanical layer a clear build-up drawing including all copper layers, soldermask and legend layers, in the correct sequence and with the correct corresponding data file name.
- Include a simple ASCII text file with your data indicating which file is to be used for which layer, preferably already in the correct build-up sequence (this is the least preferred solution: it is better if the build-up is indicated in the Gerber data as in the previous 3 suggestions).

9. RECOMMENDATION. If holes on inner layers are not connected on a particular layer, do not give them a pad in the inner layers. In any case we will remove all unconnected pads on the inner layers.

10. Thermal definition: make sure your thermal relief pads are properly defined and comply with the chosen pattern classification for Annular Rings (AR), Track Widths (Thermal Segment Width) and Gaps.

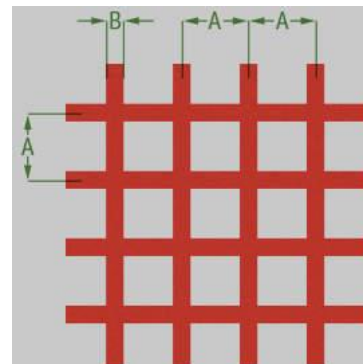


Good practice for Thermals is to work with a Gap of 0.20mm and a Thermal Segment Width of 0.20mm.

11. Hatching patterns. RECOMMENDATION: use full copper rather than hatching patterns in copper planes.

If you need a hatching pattern, then use following minimum settings:

- Minimum distance center to center between tracks of pattern (A): 0.60mm
- Minimum track width for pattern (B): 0.20mm



IMPORTANT:

Any hatching pattern that **DOES NOT meet** these minimum requirements will be converted into a full copper plane.

BGAs

Designers sometimes ask us for some guidelines on BGAs. Independent of particular components you need to consider what size of pads you need to use and how many connections you need to bring out of the package.

For the ElektorPCBService you need to bear in mind that the minimum track to track and track to pad isolation is 0.150 mm, the minimum track width is 0.150 mm and the smallest finished hole size is 0.25 mm if you want vias under the device. For a 0.25 mm finished hole size the smallest pad we need for a good annular ring is 0.600 mm on outer layers and 0.700 on inner layers.

Mechanical layer

1. RECOMMENDATION: Do ALWAYS include a Gerber mechanical layer in your data set.

IMPORTANT:

- A proper mechanical layer is **VITAL to a good and flawless production** of the PCB as it should provide us with all the needed mechanical information for the construction of your PCB.
- In case of **cut-outs or slots** in your PCB, this layer is essential to the production!
- **DO NOT scale** your mechanical layer, it should be 1 to 1 and reflect the exact dimensions of the PCB.
- The mechanical layer is – as for all layers – also **viewed from top to bottom through your PCB**, so no mirroring of the mechanical layer.
- **ONLY** include information in your mechanical layer that is needed

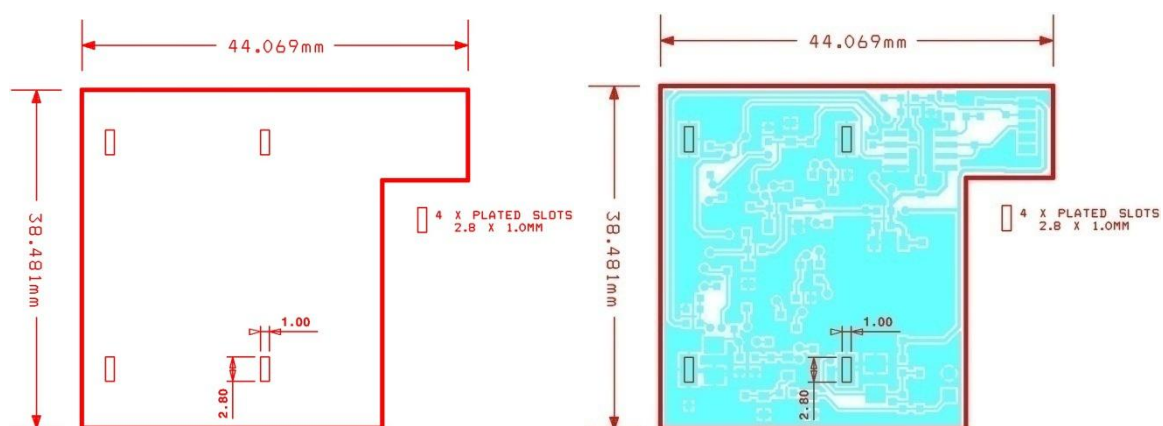
2. **Do not provide actual routing layers** for board contours or inside milling.

Routing data is production-specific depending on the rout tools, tool compensations, routing order and direction used by each PCB fabricator. This means that we cannot use customer-provided routing layers. We need to completely rework them, which can lead to confusion and misinterpretations which may result in incorrect boards.

It is our job as board producers to prepare correct production routing layers based on the information in your mechanical layer

3. A mechanical layer should **MINIMALLY contain:**

- The exact board outlines, ideally including dimensions.
- Exact positions and sizes for all inside milling, slots or cutouts, ideally including dimensions.



Outlines are best shown using a small line (e.g. 0.50mm wide) where the center of the line represents the exact board outline.

IMPORTANT:

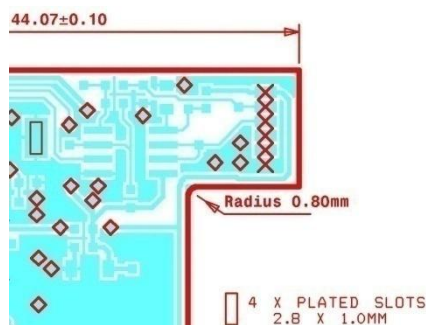
When no dimensions are given we will always take the center of the contour lines to be the exact outline of the board, regardless of their thickness.

4. Additional information that **should be included** in the mechanical plan **when needed**:

- A **reference hole**: the distance from one drill hole in X and Y to the PCB outline. This is particularly important when you only have NPTH holes without copper pads.
- **PTH/NPTH indication** for holes and slots
- A clear **layer sequence or buildup drawing** including all copper layers, soldermask and legend layers, any additional layers like peel-off or carbon, in the correct sequence viewed from top to bottom and with the correct corresponding data file name.
- **Panelised data are considered as a single board**, we do not provide separation of the individual boards by means of break-routing, scoring (V-cut) or any other separation method .

5. The standard tool size used for all outline routing is 2.00mm.

This means that the standard minimum radius for inside corners is 1.00mm.



Requirements for a smaller radius on inner corners should be clearly indicated in the mechanical layer.

DESIGN TIP:

A sharp or 90 degrees inner corner can be obtained by placing a properly sized NPTH drill exactly on the board outline center of the inner corner or by a clever design of your board outline.



6. Standard mechanical tolerances.

Routed boards

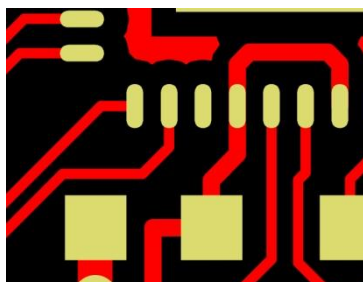
Tolerance on contour dimensions	+/- 0.20mm
Tolerance on position of contour/cutouts to holes	+/- 0.20mm
Tolerance on slot dimensions	
Width	+/-0.10mm
Length	+/-0.20mm

Soldermask

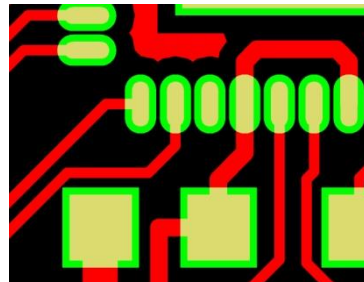
1. When generating output data for soldermask, **there is no need to oversize or compensate the soldermask pads.**

It is better to leave the soldermask pads at the same size as the copper pads. We will then set the soldermask to suit the technological needs for proper production and assembly of the boards.

Preferred version without oversizing

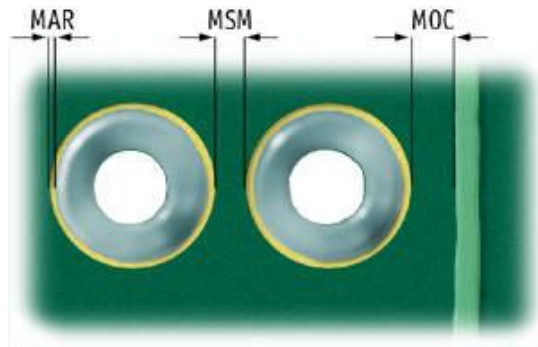


Less good: pads are oversized



2. Soldermask preparation rules that we use:

We set the values for soldermask preparation according to the PCB pattern class. The different features are shown in the diagram:



MAR (Mask Annular Ring) – the clearance between the soldermask and the copper pad

MSM (Mask Segment) – the bridge of soldermask between adjacent pads

MOC (Mask Overlap Clearance) – the soldermask cover between a track or plane and an adjacent soldermask window

We always start by applying the standard values to the complete soldermask. Depending on the design we can reduce these standard values at particular places down to the minimum accepted values to generate the best soldermask.

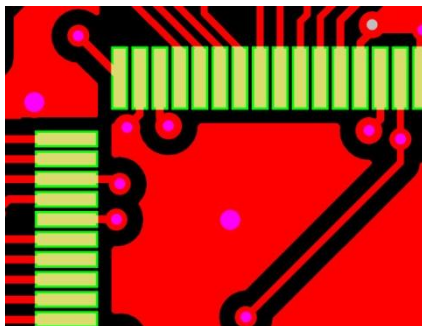
The **standard value** for MAR, MSM and MOC is **0.1000mm for all pattern classifications**.

The **MINIMUM accepted** values for MAR, MSM and MOC depend on the pattern classification according to the following table

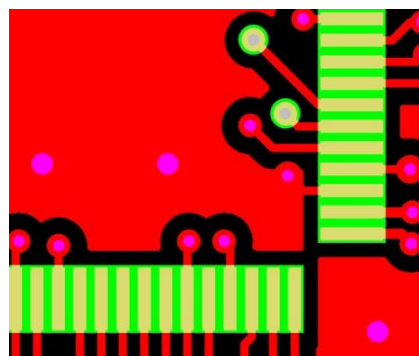
	MAR Mask Annular Ring	MSM Mask Segment	MOC Mask Overlap Clearance
Standard Value	0.1000	0.1000	0.1000
Minimum accepted values depending on Pattern Classification			
Pattern Classification	MAR Mask Annular Ring	MSM Mask Segment	MOC Mask Overlap Clearance
3	0.0800	0.1000	0.1000
4	0.0600	0.1000	0.1000
5	0.0600	0.1000	0.1000
6	0.0600	0.0800	0.0750

IMPORTANT:

- Mask Segments smaller than 0.0800mm will be removed.



→ This will be converted to the image below if the Mask Segment (MSM) between the pads is less than 0.0800mm



- For **NPTH drills without copper pad** the Mask Annular Ring (MAR) is **ALWAYS 0.125mm** independent of the pattern class.

3. **Tented via's: the copper pad of the via is covered with soldermask.**

IMPORTANT: If you require tented vias please make sure that you generate your soldermask data without soldermask pads for vias.

Tented via technology DOES NOT automatically mean that the via hole is fully closed or covered with soldermask. The maximum via ENDSIZE that can be closed with soldermask is 0.25mm.

4. NPTH holes without copper pad should ALWAYS have a soldermask clearance pad.

5. When generating output include the board outline in your soldermask layers. This is best done using a small line (e.g. 0.50mm wide) where the center of the line is the exact board outline. We will remove the line from the final production ready data.

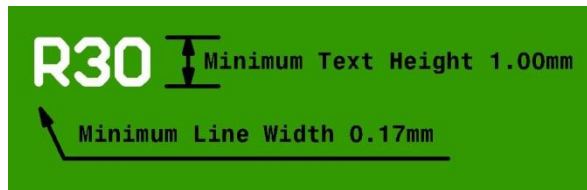
IMPORTANT:

If you require board edge areas of your PCB to be free of soldermask, use a wide line to indicate the board outline. The line-width should be at least 2.00mm, resulting in 1.00mm soldermask-free border. It is also advisable to indicate the soldermask-free border in the mechanical plan.

Legend Print

1. Specifications for Legend Print:

- Minimum Legend Line Width: 0.17mm
- Minimum Text height for good readability: 1.00mm.



2. The Legend Print will **ALWAYS be broken – or clipped – against the corresponding soldermask layer.**



Clipping rules:

- Legend clipping clearance is 0.10mm. This means that we clip the legend 0.10mm back from the soldermask openings.
- Any bits of line smaller than 0.17mm are removed.

In absence of a soldermask layer, the legend print is clipped against the corresponding copper layer. If there is no copper layer, the legend is clipped against the drill layer.

DESIGN TIP:

To avoid your legend being clipped maintain a minimum distance of 0.20mm between your legend elements and the copper image (0.20mm = 0.10mm Soldermask Annular Ring + 0.10mm Legend Clipping Clearance).

3. All legend text must be correctly readable.

As a **PCB is always viewed from top to bottom through the PCB**, text on the top layer of your board should be readable and text on the bottom layer should be non-readable or mirrored.

4. Include the board outline in your legend layers output data.

This is best done using a small line (e.g. 0.50mm wide) where the center of the line is the exact board outline. This line will be removed by us from your design.

In all cases we will clip away any legend text within 0.25mm of the board edge.

5. It is **NOT ADVISABLE** to place a legend layer on the copper layer side of a PCB without soldermask layer.

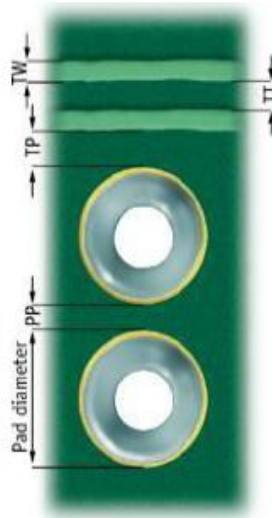
January 2009

ElektorPCBService PCB Classification

Pattern Class	class 3	class 4	class 5	class 6
min X	0,300	0,250	0,200	0,150
min Y	0,200	0,150	0,150	0,125
min Z	0,200	0,200	0,200	0,175

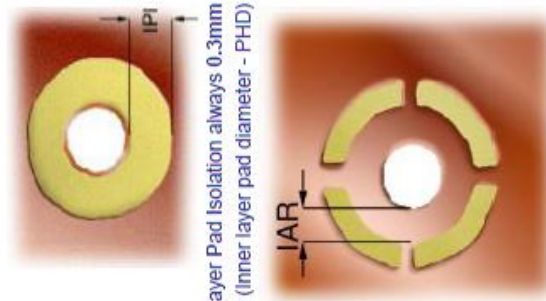
The smallest value (X, Y or Z) determines the **Pattern Class** of the board

X : smallest of the minimum values of TT-TP-PP-TW

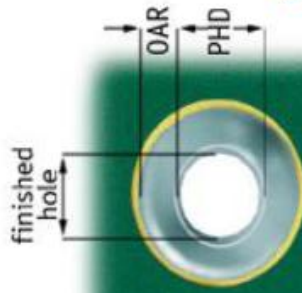


Y : smallest OAR (Outer layer Annular Ring = 1/2 (outer layer pad diameter - PHD))

Z : smallest IAR (inner layer Annular Ring = 1/2 (inner layer pad diameter - PHD))



Note: Inner layer Pad Isolation always 0.3mm
IPI = 1/2 (inner layer pad diameter - PHD)



Smallest **PHD**: Production Hole Diameter or tool size = finished hole size + 0.15 mm
 + 0.10 mm for Plated Through Holes (>=0.45mm)
 + 0.05 mm for vias (finished hole size <=0.45mm)

Drill Class	class A	class B	class C
min PHD	0,65	0,45	0,35
Corresponding finished hole size			
PTH	0,50	0,35	0,25
NPTH	0,60	0,40	0,30

The smallest value (**PHD**) determines the **Drill Classification** of the pcb

Generating Gerber & Excellon data files in Eagle

Generating Gerber- and Excellon files in Eagle (V 5.6.0) is a piece of cake. Simply follow these steps:

1. Open the CAM Processor
2. Select under File -> Open for Job.
3. In the window that now opens you select the correct .cam-file, in this case gerb274x.cam (in the Eagle subdirectory cam). For a 4-layer PCB select gerb274x-4layer.cam.
4. The job opens itself in the CAM processor window. In the right-hand panel the necessary items are already selected. You do not need to do anything here.
5. Activate in **every (!)** layer the Dimension by clicking on it. This shows the outline of the PCB. The tick box next to Mirror needs to be un-ticked each time.
6. The final step is carrying out the job. This is simply done by clicking the button Process Job.
7. The CAM Processor places the Gerber files in the folder of your opened project. There are quite a few files there (six for a two-layer board).
8. To create an Excellon file that contains the information for drilling the holes, you select the excellon.cam file when opening the .cam-file (steps 2 and 3). You then click process job and the Excellon file will be generated. You now simply combine all these files into a single zip file and upload it via the Elektor PCB Service website.